IN THE CLAIMS

Please amend the claims as shown below.

1. (Currently Amended) A high voltage device formed in a region of a silicon substrate of a first conductivity type delimited by a wall of a second conductivity type, comprising:

a lower surface comprising a first region of the second conductivity type connected to the wall.

an upper surface comprising a second region of the second conductivity type,

a high voltage being likely to exist between the first and second regions and having to be withstood on the upper surface side by a junction between the second region and the substrate or by a junction between the wall and the substrate,

a conductive track being likely to be at a high potential extending over the substrate between the second region and the wall, and

a third region of the first conductivity type of a high doping level formed in the substrate under a portion of the track substantially halfway between the second region and the internal periphery of the wall, the third region being contacted by a field plate which is insulated from the track, and extends widthwise at least substantially across the track and lengthwise beyond the third region on either side of the third region in the direction of the wall and of the second region.

2. (Previously Amended) The device of claim 1, wherein the field plate extends beyond the third region in the wall direction and in the direction of the second region over a distance greater than 10 μm.

3. (Previously Amended) The device of claim 1, wherein the external periphery of the second region comprises a ring of the same conductivity type as the second region, but having a lower doping level than the second region.

4. (Currently Amended) A high voltage device formed in a region of a silicon substrate of a first conductivity type delimited by a wall of a second conductivity type, comprising:

a lower surface comprising a first region of the second conductivity type connected to the wall;

an upper surface comprising a second region of the second conductivity type;

a conductive track extending over the silicon substrate between the second region and the wall;

a third region of the first conductivity type having a high doping level formed in the substrate under a portion of the conductive track approximately halfway between the second region and an internal periphery of the wall; and

a field plate which is insulated from the track and extends widthwise at least substantially across the track and lengthwise on either side of the third region, beyond the third region, in the direction of the wall and of the second region, at least a portion of the field plate being in contact with the third region.